

VER : 1A

ZQ2B SOLE UMA SYSTEM DIAGRAM



Danube Platform
(Main Stream)

BOM P/N	Description	Model	SidePort	ODD
31ZQ2MB00A0	ZQ2B 6L JM MB (W/GRN,SAM,W/O CPU)ASSY	JM	Samsung	Slim
31ZQ2MB00E0	ZQ2B 6L JM MB (W/GRN,HYU,W/O CPU)ASSY	JM	Hynix	Slim
31ZQ2MB00H0	ZQ2B 6L JV MB (W/GRN,W/O CPU,VRAM)ASSY	JV	No Support	Standard

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

IV @ ----> iGPU
SP @ ----> Option Notice
SIDE @ ----> SidePort VRAM
GA @ ----> Green Adapter (Default stuff)

Sideport-L75,L76,R583,R392,C832,R455,R550,R502
NB A11-R105,R108
SB A12-R267,R271
JV/JM-CN16,R450,R456
EC-D8,D27
UMA-R461
VRAM-R358,R359,R360,R363,R365,R72

CHARGER (ISL8731A) PAGE 26

AMD CPU CORE (ISL6265) PAGE 28

NB_CORE (UP6111AQDD) PAGE 30

0.9V/DDR 1.5V(RT8207) PAGE 31

SYSTEM 5V/3V (RT8206) PAGE 27

1.1V(UP6111AQDD) PAGE 29

Discharge /Thermal protec PAGE 32

DDR3- SODIMM1
PAGE 5

DDR3 channel A

AMD Champlain
S1G4 Processor
35mm X 35mm
638P (PGA) 35W
PAGE 2,3,4

CPU THERMAL
SENSOR
(Reserve Only)
PAGE 4

PWM FAN SCH.
PAGE 24

CPU (PROCHOT)
E.C.(CPUFAN#)

CPU SideBand TemperatureSense I2C

HT3
1.8GHz

CPU_CLK
NB GFX_CLK
NB GPP_CLK
SBLINK_CLK

From SB
CLK GEN

SB820M
PAGE 10

CLK_PCL_775

PCLK_DEBUG

25MHz

LAN
Atheros
PCIe-LAN
AR8151
(10/100/1000)
PAGE 17

Mini PCI-E
Card
(Wireless LAN)
PAGE 18

NORTH BRIDGE
RS880M
A11
21mm X 21mm, 528pin BGA
GFX Engine: 500MHz
TDP: 13W
0.95 ~ 1.1V
PAGE 6,7,8,9

gDDR3 VRAM
DDR III-800MHz PAGE 6

HDMI PAGE 16

CRT PAGE 15

LVDS PAGE 23

A-LINK

SOUTH BRIDGE
SB820M
A12
23mm X 23mm, 605pin BGA
TDP: 4.9W
PAGE 10,11,12,13, 14

SATA - HDD
PAGE 19

SATA0 150MB
3 Gb/s

SATA - ODD
PAGE 19

SATA1 150MB
3 Gb/s

USB2.0 Port
on board x1
PAGE 30

Blue Tooth
PAGE 22

Web-Camera
PAGE 15

USB BOARD
USB2.0 Ports x3
PAGE 22

Mini Card
WLAN & Debug
PAGE 18

CardReader
AU6347
PAGE 21

Power BOARD
PAGE 22

Switch BOARD
PAGE 22

There are three Daughter boards.

CPU SideBand TemperatureSense I2C

CLK_PCL_775

Winbond KBC
NPCE781L &
Green Adapter
PAGE 25

Audio CODEC
RTL ALC271X
PAGE 20

Green ADP.
PAGE 25

Keyboard
TouchPad
PAGE 24

SPI ROM
PAGE 25

Digital MIC
PAGE 15 & 20

AUDIO CONN
(H.P./ MIC)
PAGE 20

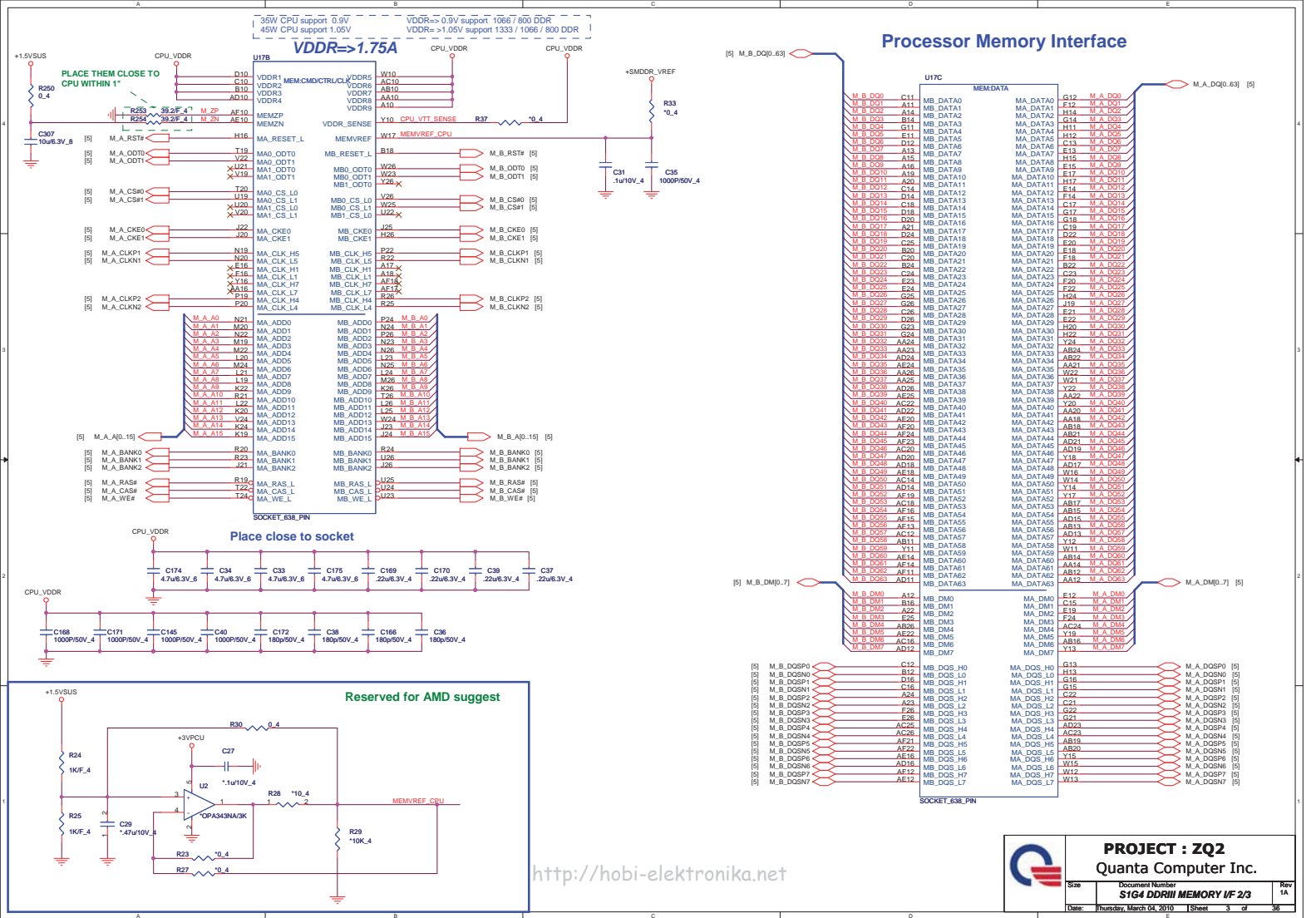
Speaker CN
PAGE 20

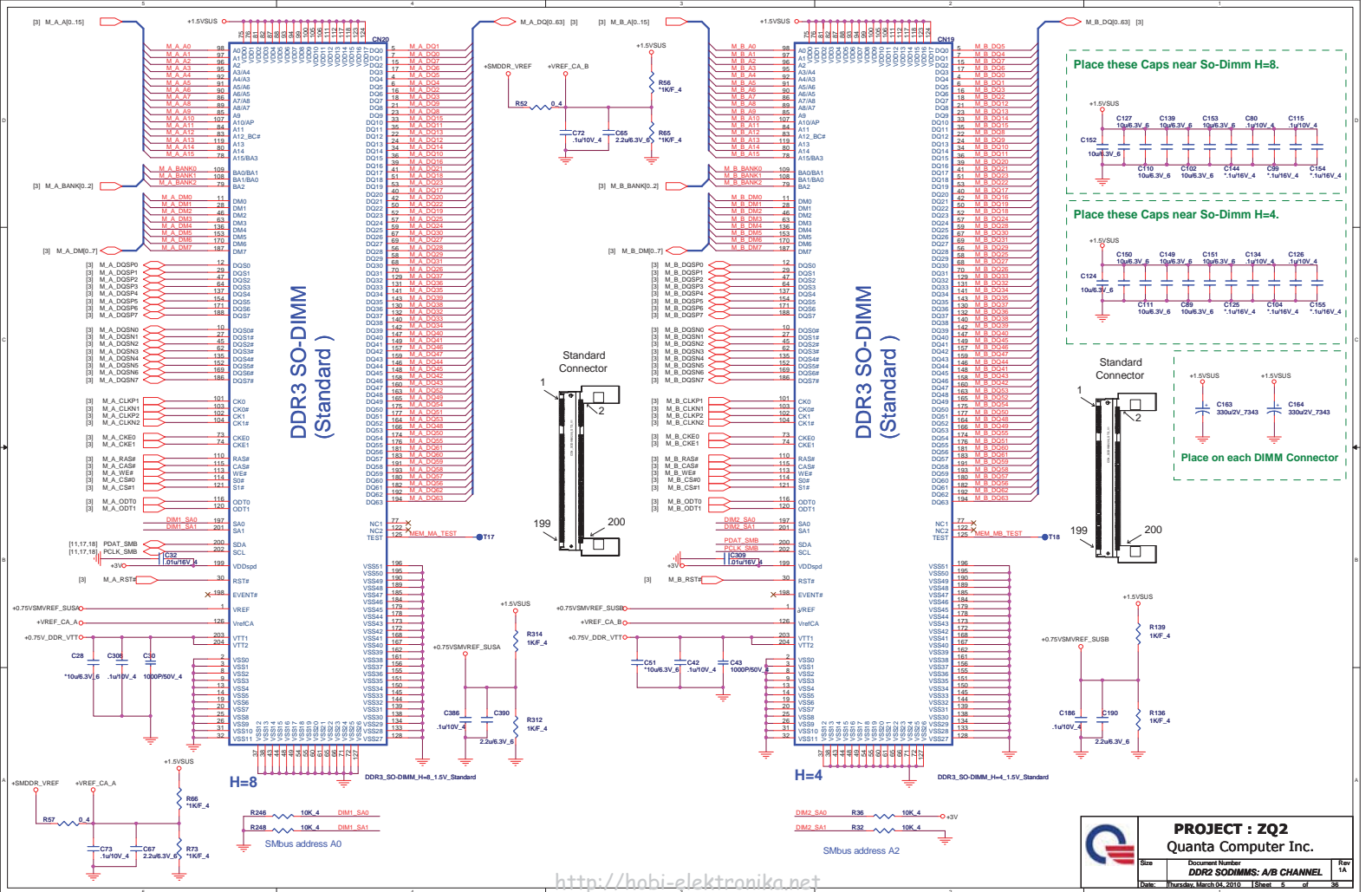
SSID: 035E
SVID: 1025



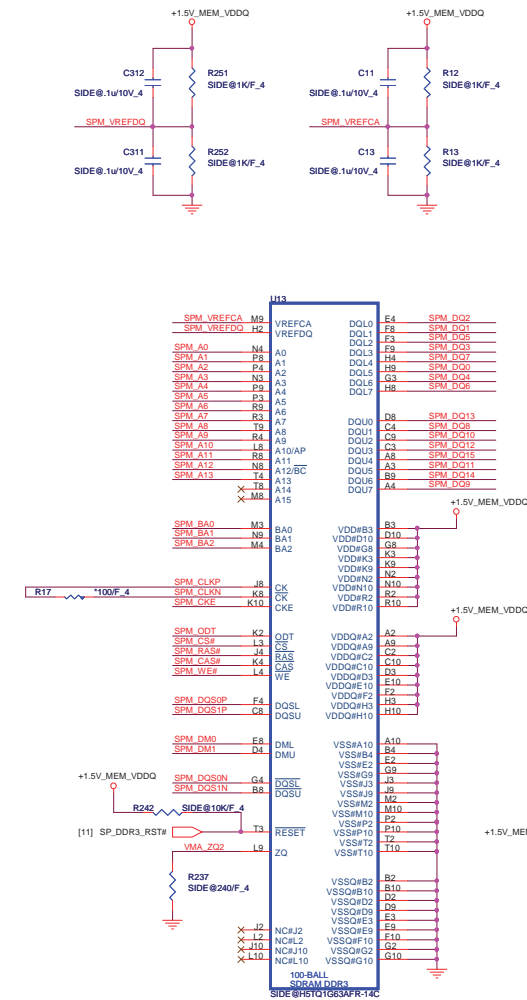
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
Date:	Thursday, March 04, 2010	Sheet 1 of 36





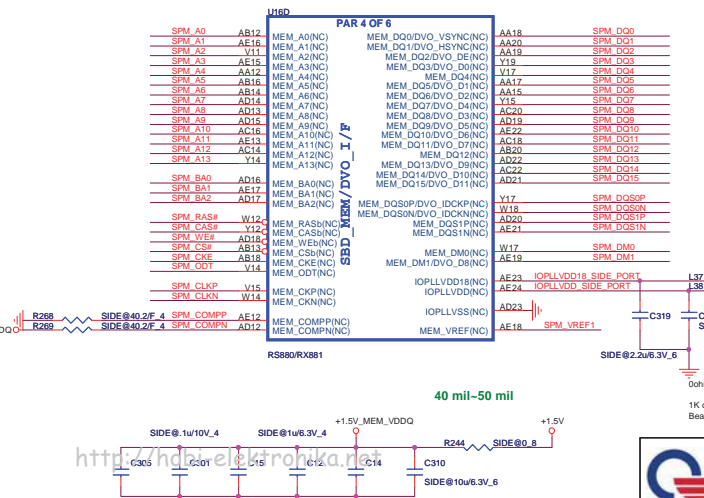
SIDE PORT



Signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

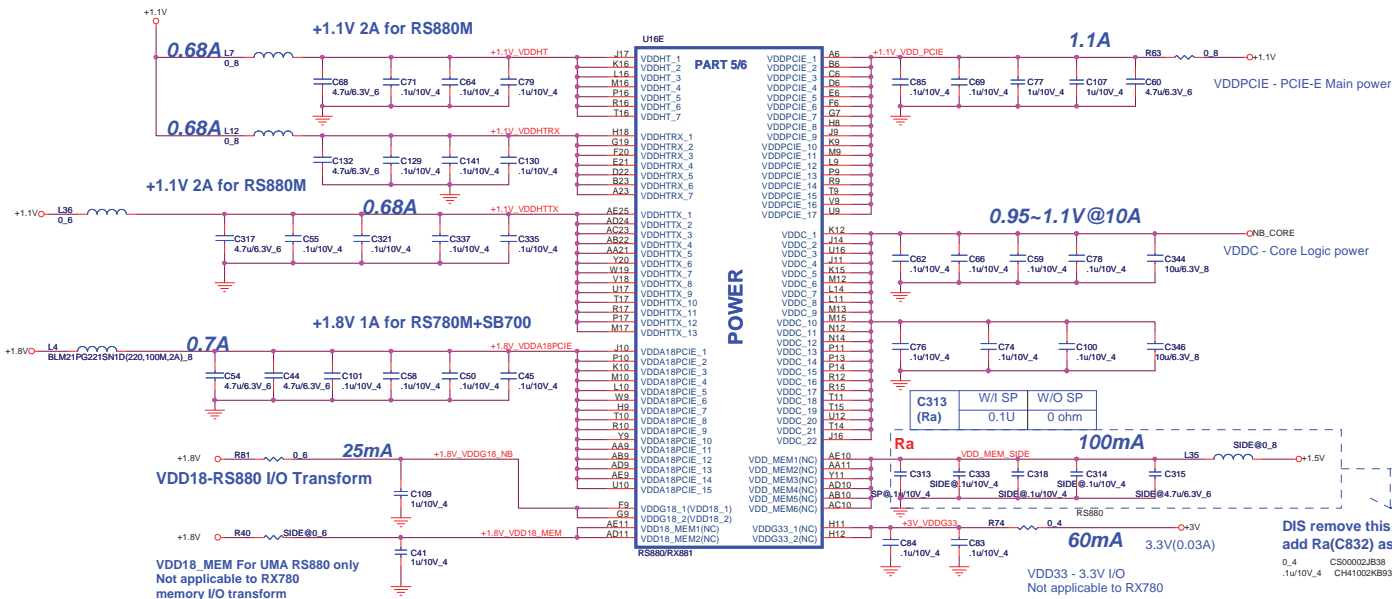
RES CHIP 1.21K 1/16W +1% (0402)
P/N : CS21212F18

This block is for Side-Port only



	W/T SP	W/O SP
R266	1K	0
L37	Bead	0
L38	Bead	0

PROJECT : ZQ2
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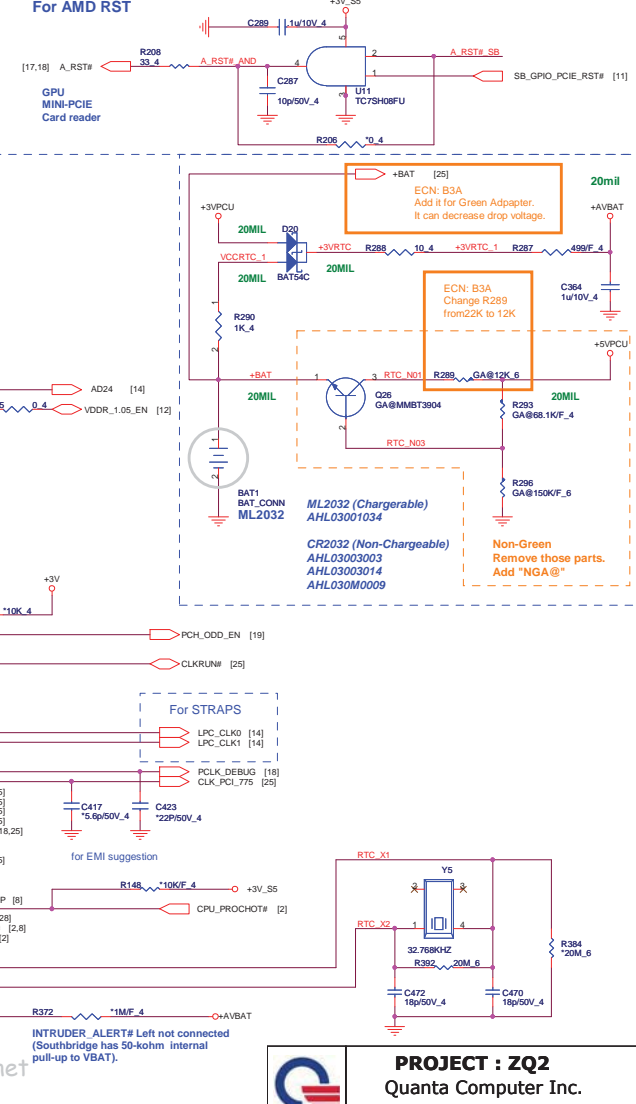
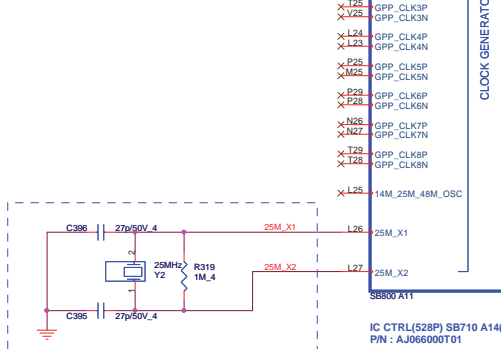


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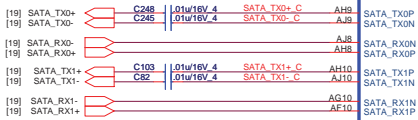
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number RS880M-POWER4/4	Rev 1A
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Max trace length: 6"

SATA HDD

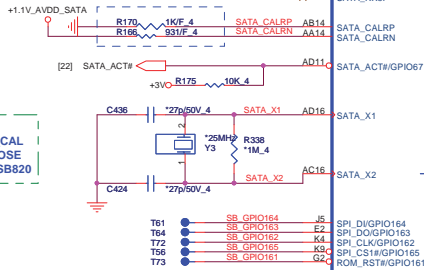


SATA ODD

SATA PORT 0,1,2,3 can support AHCI mode

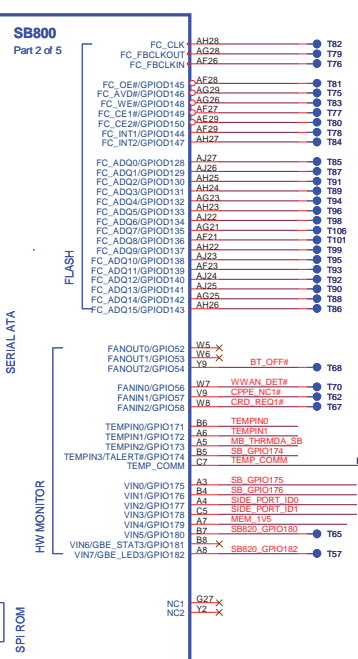
Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. SB800 A12: 1K ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931 ohm 1% resistor to VDDAN_11_SATA. SB800 A12: 931 ohm 1% resistor to VDDAN_11_SATA.

E-SATA

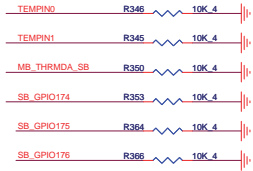


PLACE SATA_CALRES VERY CLOSE TO BALL OF SB820

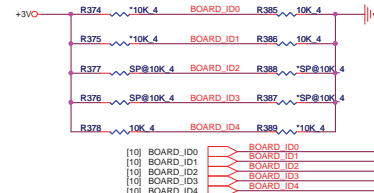
SB800 A11



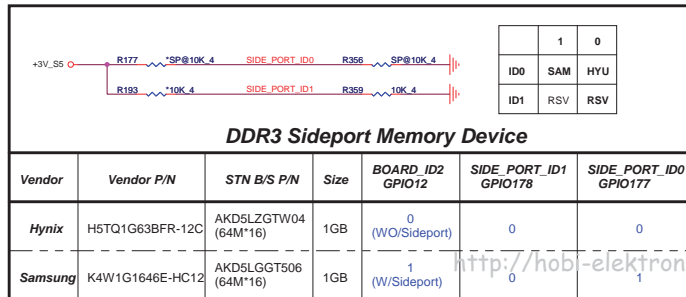
Check list



BOM check



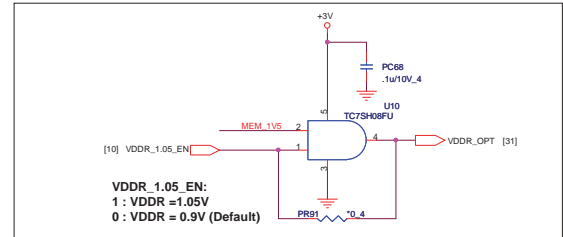
	1	0
ID0	15"	14"
ID1	DIS	UMA
ID2	W/L	Sideport W/O
ID3	JM	JV
ID4	6L	8L



	1	0
ID0	SAM	HYU
ID1	RSV	RSV

DDR3 Sideport Memory Device

Vendor	Vendor P/N	STN B/S P/N	Size	BOARD_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	0 (W/O/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	1 (W/Sideport)	0	1

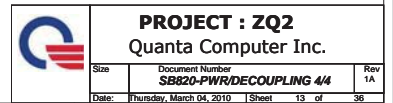


PROJECT : ZQ2
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Size	Document Number	Rev
	SB820-SATA/IDE/SPI 3/4	1A
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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

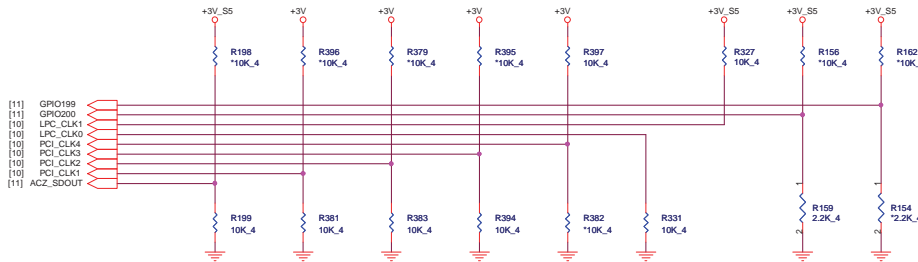
VDD-- S/B CORE power



REQUIRED STRAPS

SB820M is supported Gen.1 mode only.

For internal clock GEN.

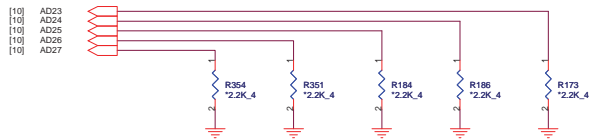


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM L, L=FWH ROM	

internal have pull Hi 10K

DEBUG STRAPS

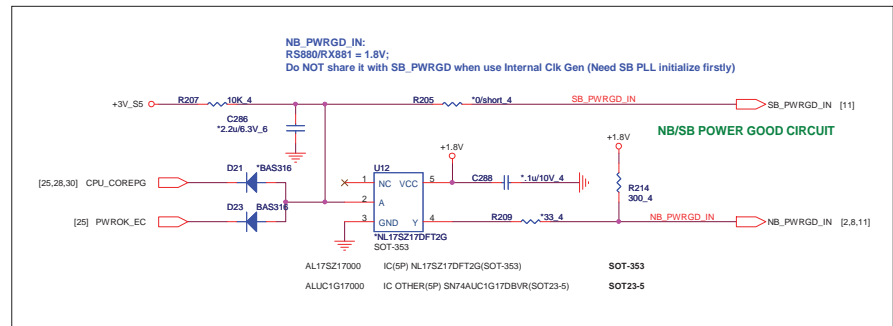
SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



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PROJECT : ZQ2
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Size Document Number
SB820-STRAPS
Date: Thursday, March 04, 2010 Sheet 14 of 36 Rev 1A

C



1



1



B

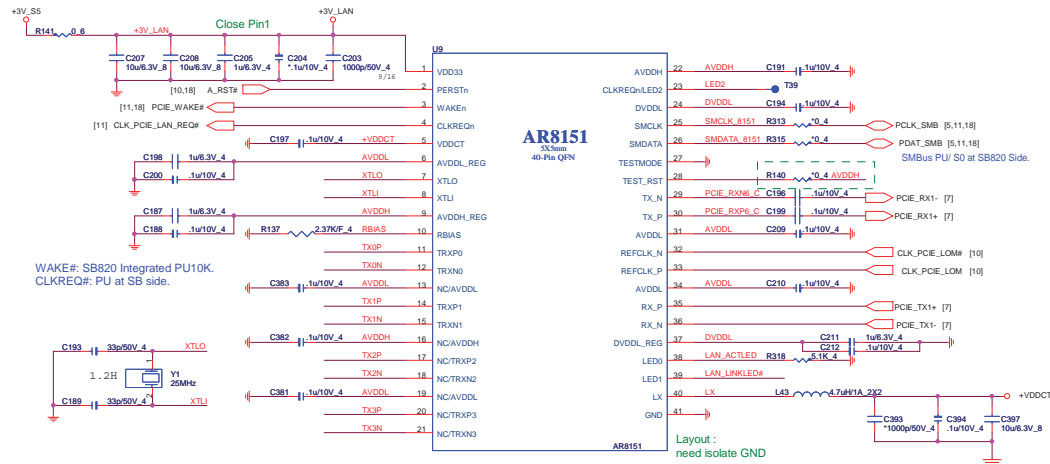
A



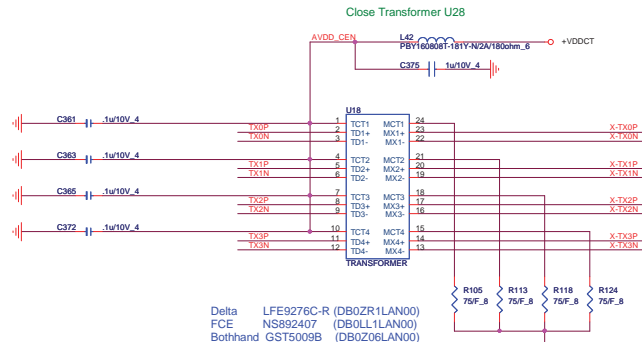
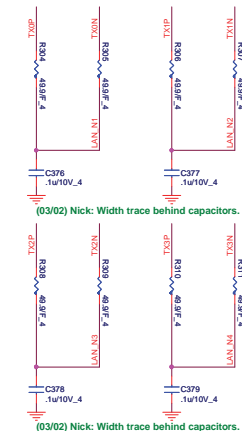
Figure 10 shows the pin connections for the HDMI module, organized into three sections: U3, U4, and U5. Each section includes a pin header with 10 pins and a *RClamp0524P pin.

- U3:**
 - Pin 1: HDMI DDC CLK
 - Pin 2: HDMI DDC DATA
 - Pin 3: GND_3/8
 - Pin 4: HDMI DET
 - Pin 5: *RClamp0524P
 - Pin 6: HDMI DET
 - Pin 7: GND_3/8
 - Pin 8: HDMI DET
 - Pin 9: HDMI DDC DATA
 - Pin 10: HDMI DDC CLK
- U4:**
 - Pin 1: TX1 HDMI+
 - Pin 2: TX1 HDMI-
 - Pin 3: TXC HDMI+
 - Pin 4: TXC HDMI-
 - Pin 5: GND_3/8
 - Pin 6: TXC HDMI-
 - Pin 7: TXC HDMI+
 - Pin 8: TXC HDMI-
 - Pin 9: TX1 HDMI-
 - Pin 10: TX1 HDMI+
- U5:**
 - Pin 1: TX2 HDMI+
 - Pin 2: TX2 HDMI-
 - Pin 3: TX0 HDMI+
 - Pin 4: TX0 HDMI-
 - Pin 5: GND_3/8
 - Pin 6: TX0 HDMI-
 - Pin 7: TX0 HDMI+
 - Pin 8: TX0 HDMI-
 - Pin 9: TX2 HDMI-
 - Pin 10: TX2 HDMI+

Giga-LAN AR8151



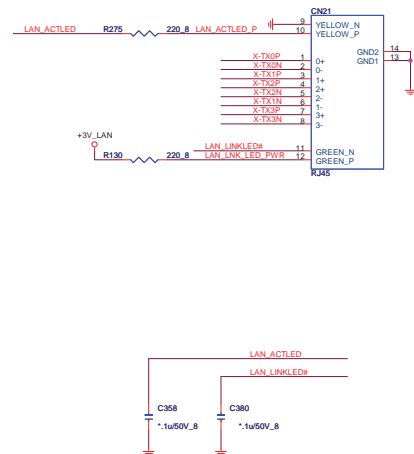
TRANSFORMER(LAN)



Delta	LFE9276C-R	(DB0ZR1LAN00)
FCE	NS892407	(DB0LL1LAN00)
Bothhand	GST5009B	(DB0Z06LAN00)

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RJ45(LAN)

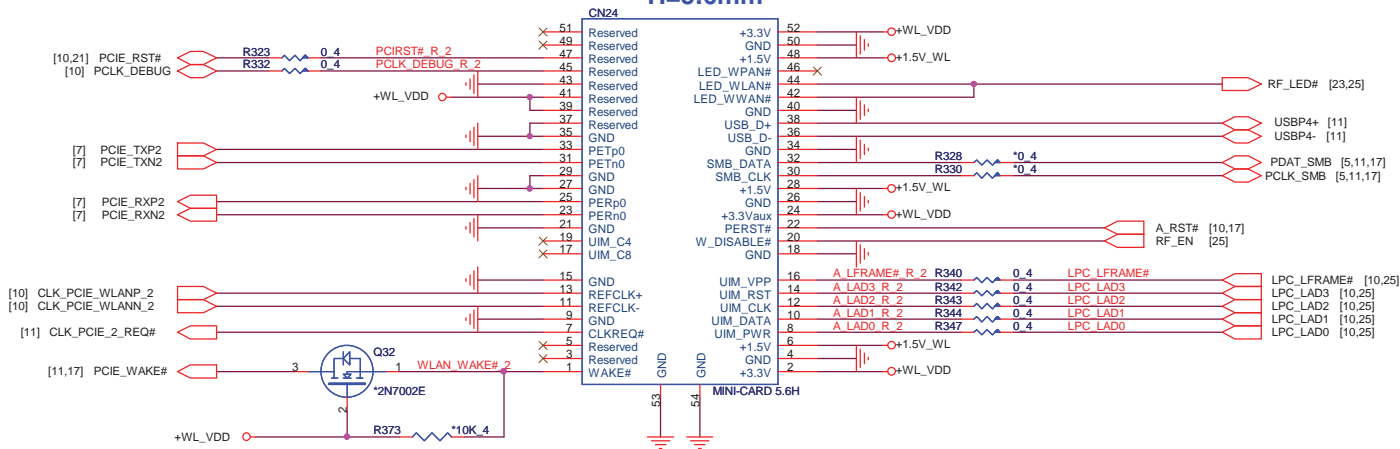


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MINI-CARD WLAN(MNC)

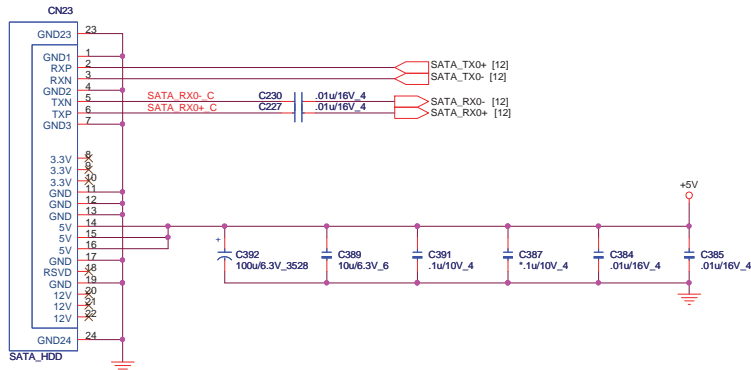
H=5.6mm



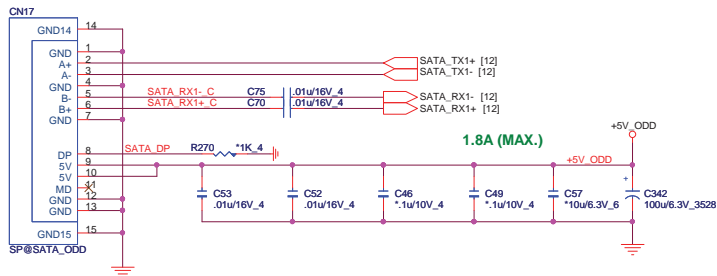
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Mini-Card/WL	1A
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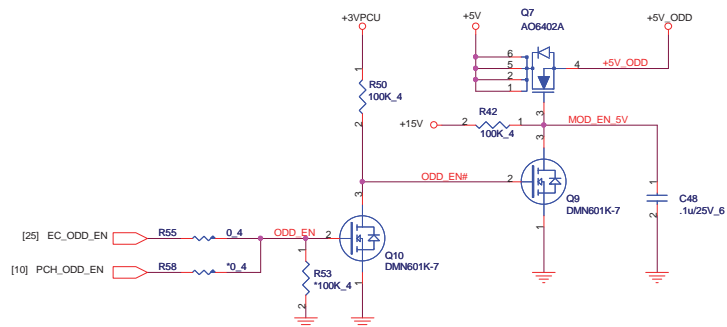
SATA HDD(HDD)



SATA ODD (ODD)



ODD POWER(ODD)



JM-9.5mm (H=2.4mm)/ Slim

Main	DFHS13FR078, DFHS13FR077
Second	DFHS13FR075

JV-12.7mm(H=5.5mm)/ Standard

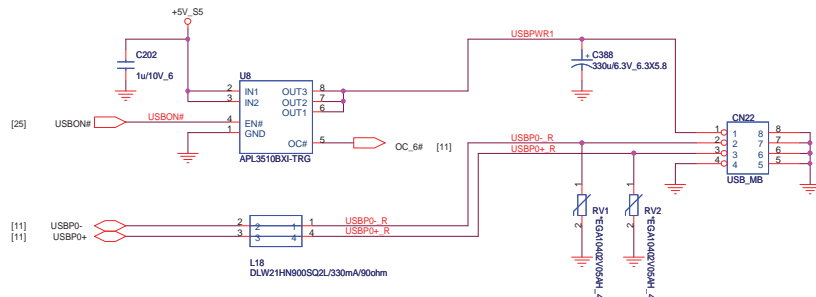
Main	DFHS13FR017
Second	DFHS13FR006, DFHS13FR005



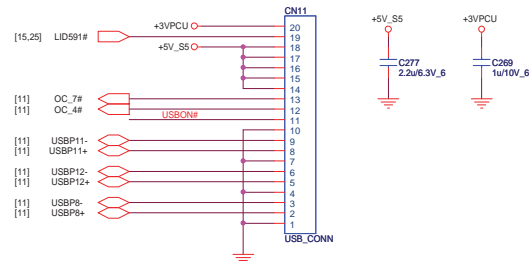
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A
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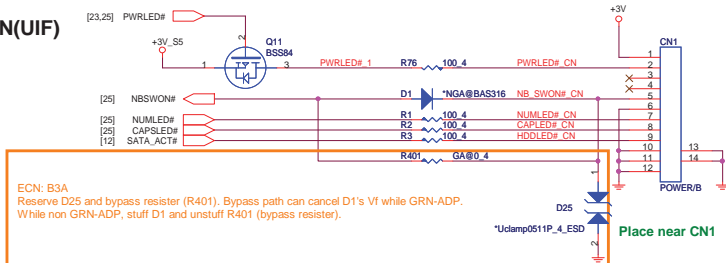
USB PORT(USB/MB)



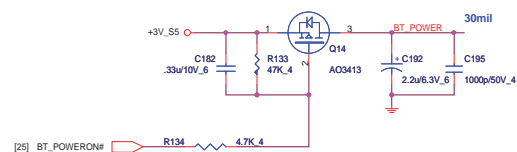
USB BOARD CONN(USB/SB)



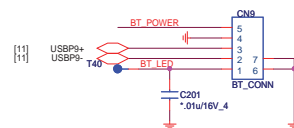
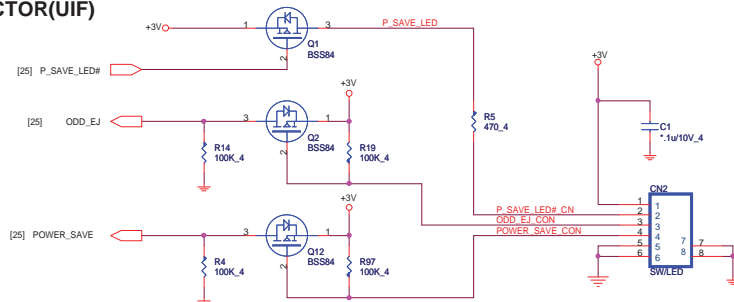
POWER BOARD CONN(UIF)



BLUETOOTH CONN(BTM)

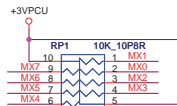


LED BOARD CONNECTOR(UIF)

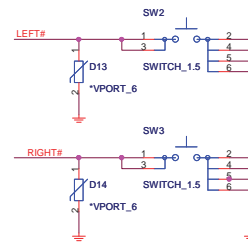


PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number USB/BT/TP	Rev 3A
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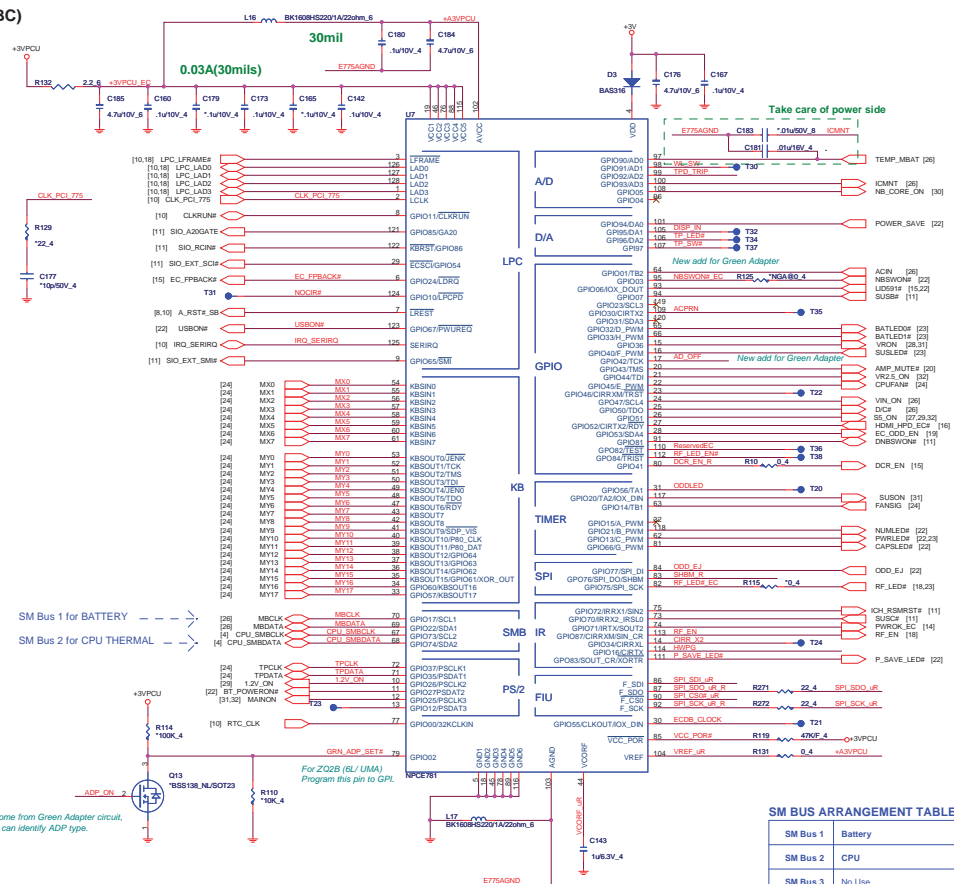
[illegible]

The schematic diagram illustrates the fan control circuit. It features two MMBT3904 transistors, Q15 and Q16, which act as switches for the fan's PWM control lines. Q15 is driven by the PM_THERM# signal (pin 2) through a 10K resistor (R222), and its emitter is connected to the FAN_PWM_E pin (pin 1). Q16 is driven by the CPUFAN# signal (pin 25) through a 10K resistor (R223), and its emitter is connected to the FAN_PWM_CN pin (pin 1). Both FAN_PWM lines are connected to the FAN connector (CN14) pins 1 and 2. The FAN connector also provides a +5V FAN supply and a GND pin. The circuit is powered by +3V and +5V rails, with various resistors (R221, R229, R224) and a 30mF capacitor (C15) shown.

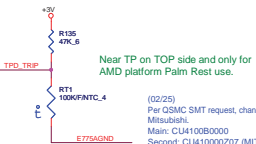
[illegible]

Size	Document Number KB/FAN/EE RETURN CAP	Rev 1A
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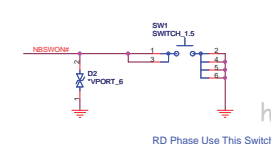
EC(KBC)



PALM REST THERMAL SENSOR (THM)




POWER-ON SWITCH (KBC)



POWER-ON SWITCH (KBC)

SHBM=0: Enable shared memory with host BIOS

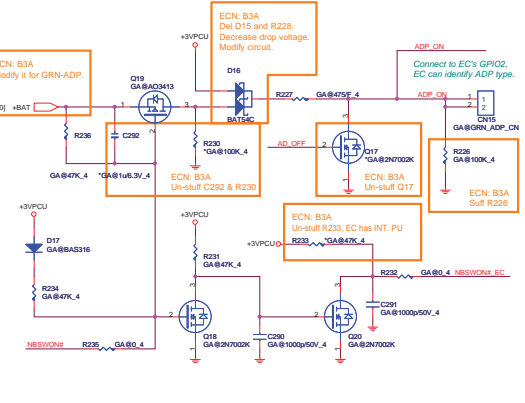


The diagram shows a circuit for the SHBM pin. A red line labeled "SHBM_R" represents the signal trace. It passes through a resistor labeled "R117" and then through a resistor labeled "10K_4". The trace then connects to a ground symbol, which is a triangle with a circle inside, representing a connection to ground.

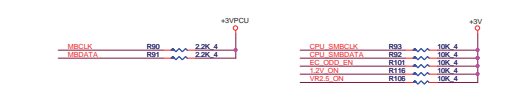
//hobi-elektronika.net

Disabled (T) if using FW H device on LPC.
Enabled (T) if using SPI flash for both system BIOS and EC firmware

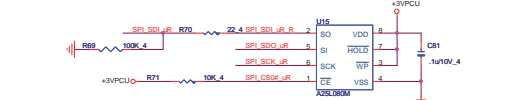
GREEN ADAPTER CIRCUIT



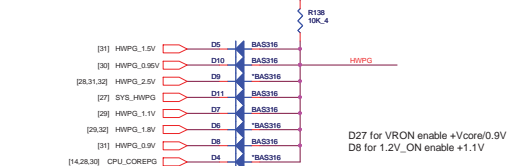
SM BUS PU(KBC)

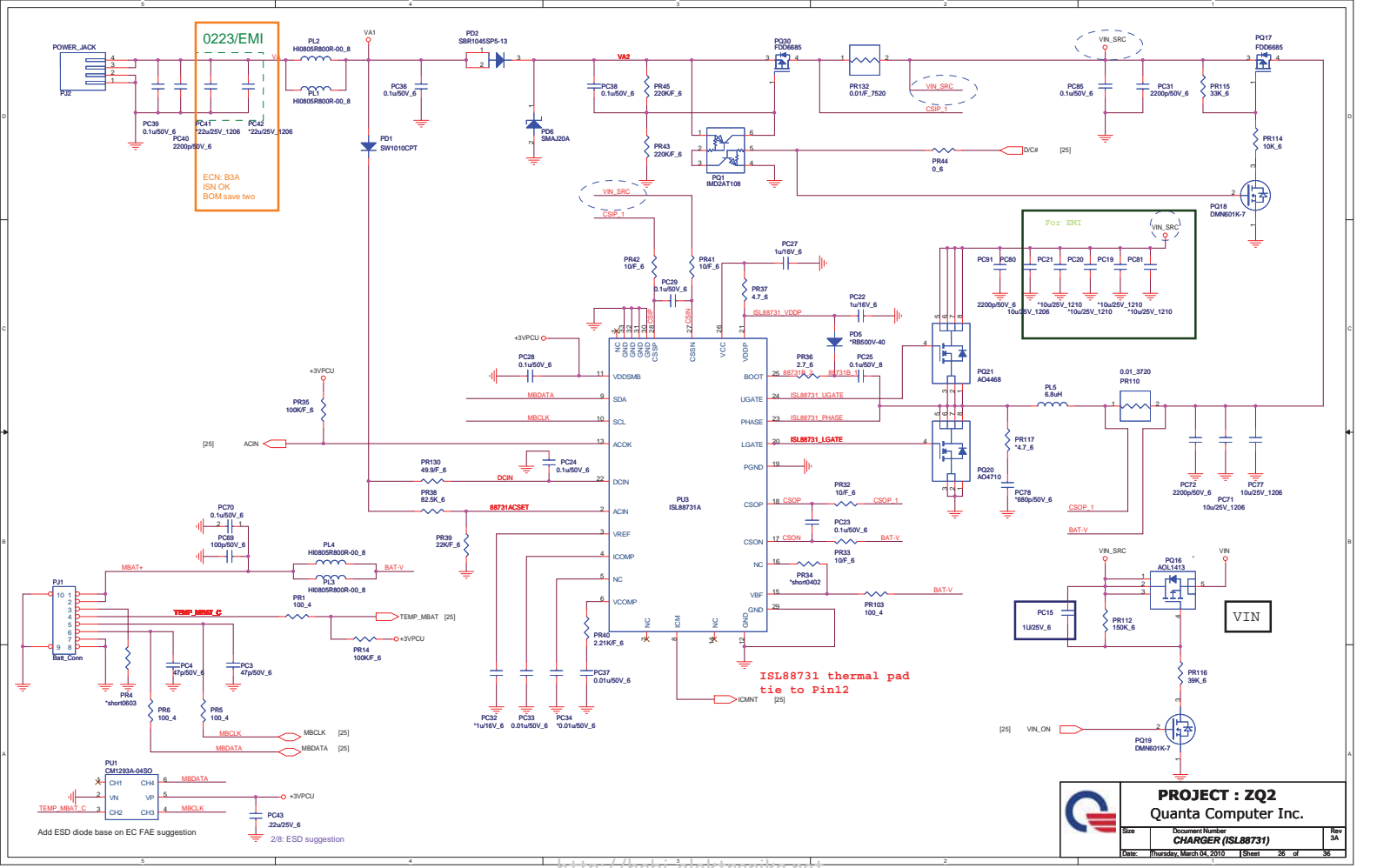


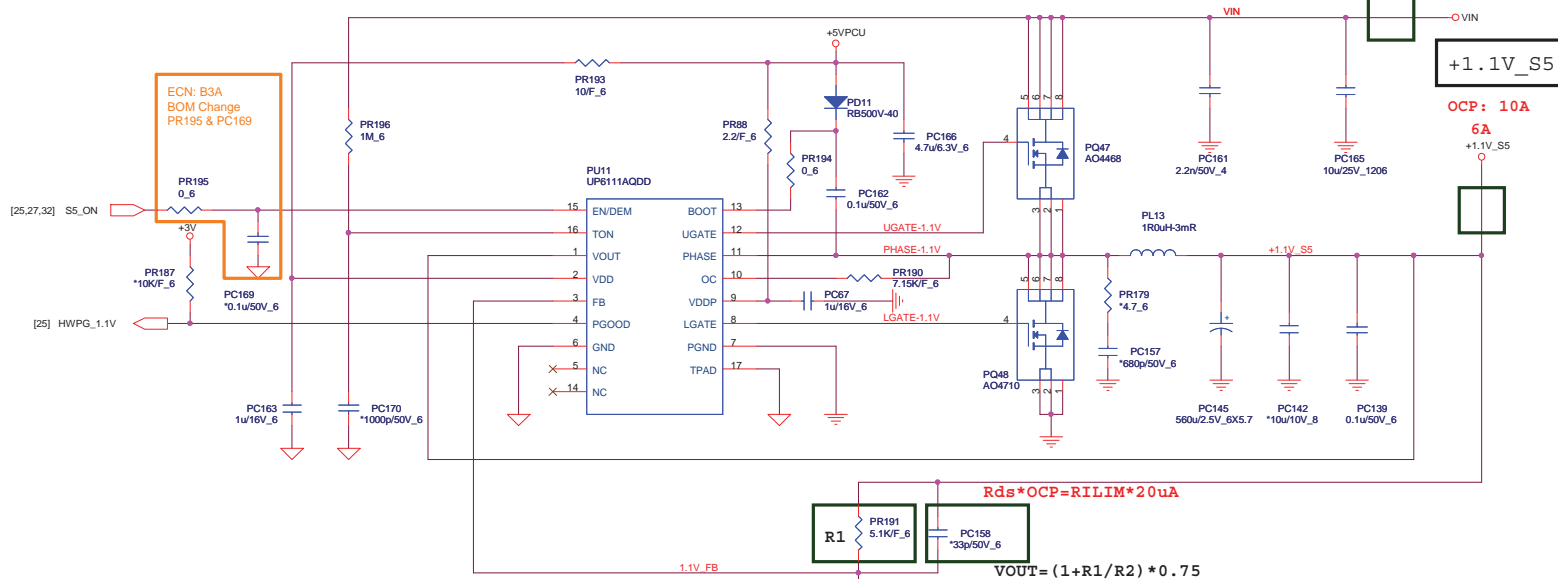
SPI FLASH(KBC)



HWPG(KBC)







$$T_{ON} = 3.85p \cdot R_{TON} \cdot V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} \cdot T_{ON})$$

$$T_{ON} = 3.85p \cdot 1M \cdot 1 / (V_{in} - 0.5)$$

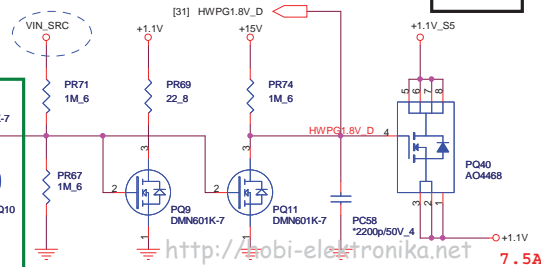
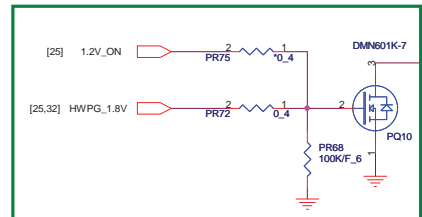
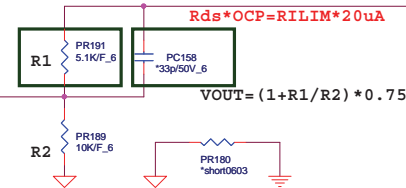
$$Frequency = 1 / (0.0036767) = 272K$$

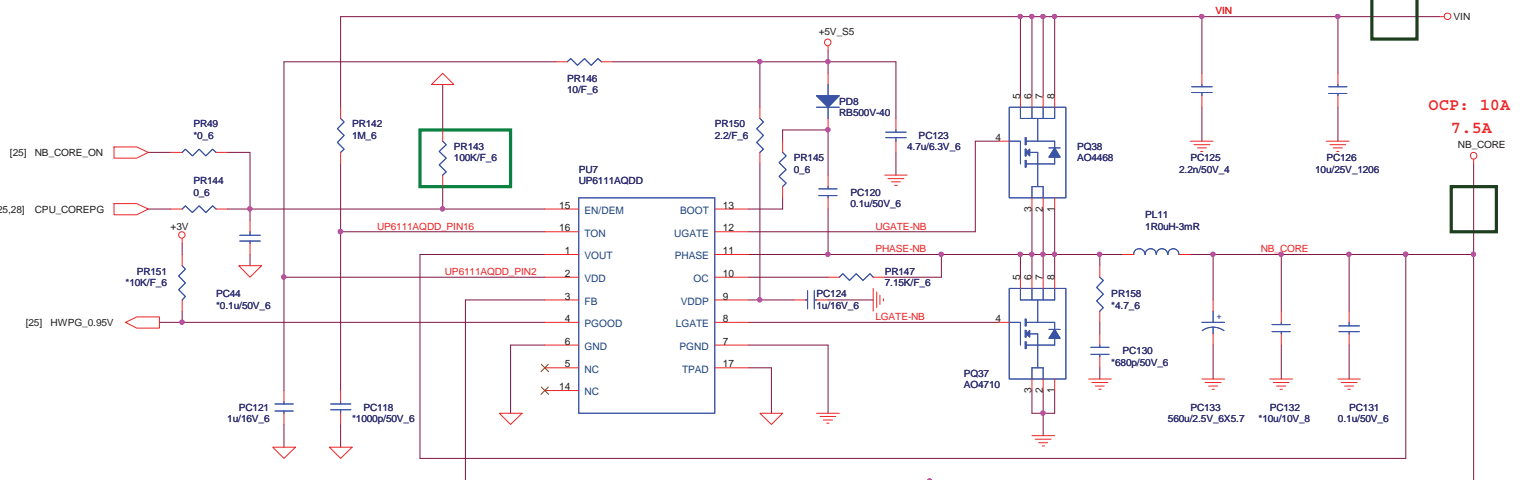
$$A04710 \quad R_{dson} = 11.7 \sim 14.2m\Omega$$

$$L(\text{ripple current}) = (19 - 1.1) \cdot 1.1 / (1u \cdot 272k \cdot 19) \sim 3.81A$$

$$14.2m \cdot 10 = R_{ILIM} \cdot 20uA$$

$$R_{ILIM} = 7.1K \sim 7.15K$$





$$VOUT = (1 + R1/R2) * 0.75$$

$$R_{ds} * OCP = RILIM * 20uA$$

$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

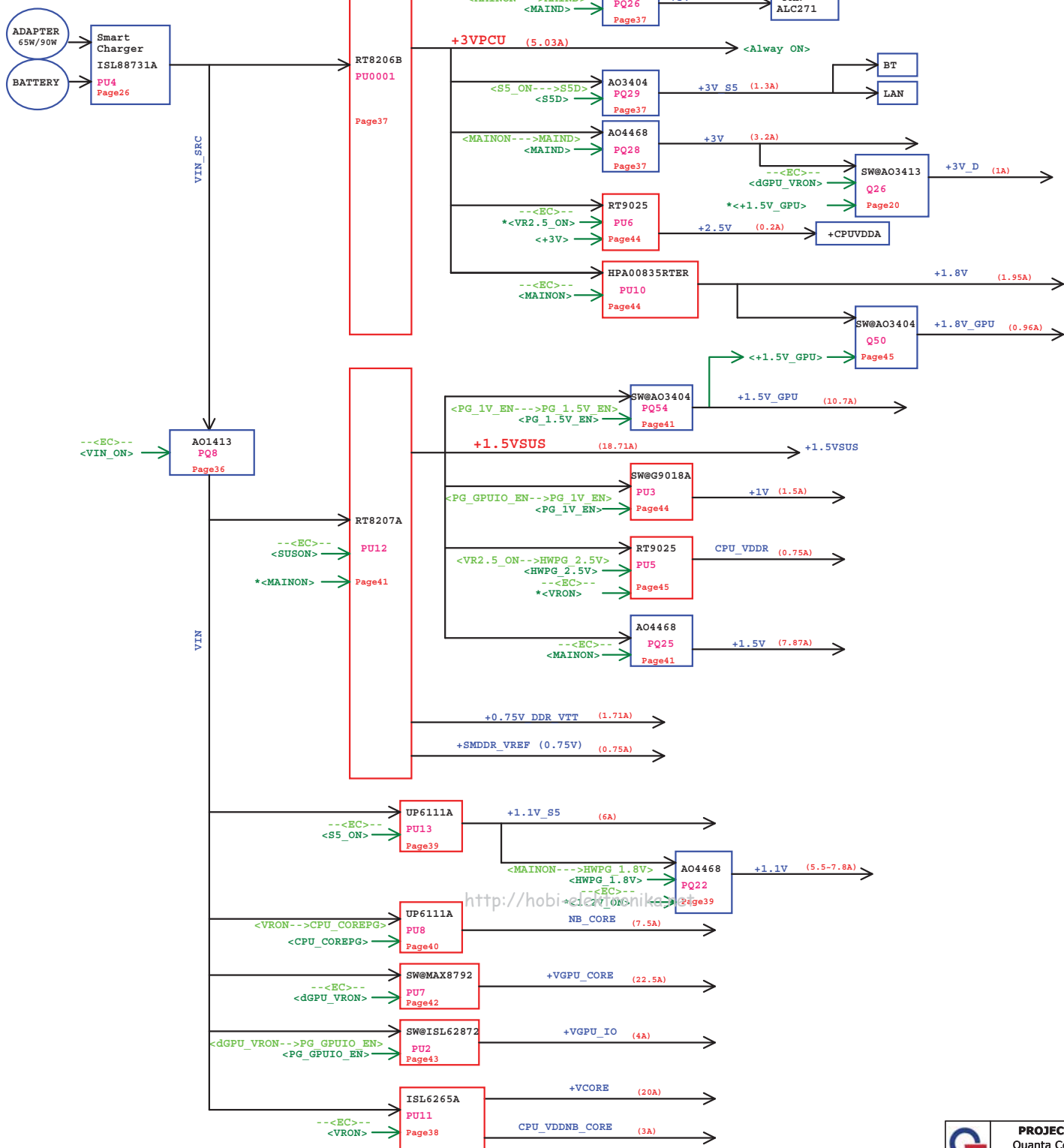
AO4710 $R_{ds(on)} = 11.7 \sim 14.2m\Omega$
 $L(ripple\ current) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.646A$
 $14.2m * 10 = RILIM * 20uA$
 $RILIM = 7.1K \sim 7.15K$

HI --- 0.95V
 LOW --- 1.1V

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev	1A
	NB_CORE(UP6111A)		
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ZQ2B Power tree



SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 3s
6, 50uS <= All power rails except +3.3V
7, 100uS <= +3.3VALW_R <= 40mS



